R65C00 CMOS Microcomputer System DATA SHEET

R65C00 MICROPROCESSORS (CPU)

DESCRIPTION

The 8-bit R65C00 microcomputer system is produced with CMOS Silicon Gate technology. Advanced system architecture enhances its performance speeds; a family of software-compatible microprocessor (CPU) devices (described below) enhances system cost-effectiveness. Rockwell also provides memory and microcomputer systems, as well as low-cost design aids and documentation.

R65C00 MICROPROCESSOR (CPU) CONCEPT

Three CPU devices are available. All are software-compatible and provide addressable memory, interrupt input, and on-chip clock oscillators and drivers options. All are bus-compatible with the NMOS R6500 family devices.

The family includes two microprocessors with on-board clock oscillators and drivers and one microprocessor driven by external clocks. The on-chip clock versions are aimed at high performance, low cost applications where single phase inputs, crystal or RC inputs provide the time base. The slave processor version is geared for multiprocessor system applications where maximum timing control is mandatory. All R65C00 microprocessors are available in a variety of packaging (ceramic and plastic), operating frequency (2 MHz, 3 MHz and 4 MHz), and temperature (commercial and industrial) versions.

MEMBERS OF THE R65C00 MICROPROCESSOR (CPU) FAMILY

Microprocessors with Internal Clock Generator:

Model	Addressable Memory
R65C02	64K Bytes
R65C102	64K Bytes

Microprocessors with External Clock Input:

Model	Addressable Memory
R65C112	64K Bytes

FEATURES

- CMOS silicon gate technology
- Low Power (4MA/MHz)
- Downward software compatible with R6502
  - —Twelve additional instructions
  - —Two new addressing modes
- Single 5V ±20% power supply
- Eight bit parallel processing
- Decimal and binary arithmetic
- True indexing capability
- Programmable stack pointer
- Interrupt capability
- Non-maskable interrupt
- Use with any type of speed memory
- Eight-bit Bidirectional Data Bus
- Addressable memory range of up to 64K bytes
- "Ready" input
- Direct Memory Access capability
- Memory Lock Output
- 2MHz, 3MHz, and 4MHz versions
- Choice of external or on-chip clocks
- On-the-chip clock options
  - —External single clock input
  - —Direct Crystal Input (÷ 4)
- Commercial and industrial temperature versions
- Pipeline architecture
- Slave Processor Version (R65C112)

ORDERING INFORMATION

ORDER NUMBER:

R65C102
R65C02
R65C112

- Temp Range
  - No Suffix = 0°C to +70°C
  - E = −40°C to +85°C
- Package C = Ceramic
  - P = Plastic
- Frequency Range
  - A = 2 MHz
  - B = 3 MHz
  - C = 4 MHz

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PRELIMINARY

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SIGNAL DESCRIPTION

Clocks (ϕ_0, ϕ_1, ϕ_2, ϕ_4)

The R65C112 requires an external ϕ_2 clock.

The R65C02 requires an external ϕ_0 clock.

The R65C102 clocks may be generated externally or internally with a crystal across XTLI and XTLO.

ϕ_0—TTL input clock to the R65C02

ϕ_4—Quadrature output clock from the R65C102. The address is valid at the rising edge of ϕ_4.

When the input clock is stopped the CPU is in the standby mode.

Address Bus (A0-A15)

These outputs are TTL compatible and capable of driving one standard TTL load and 130 pF.

Data Bus (D0-D7)

The data bus uses eight pins. This is a bidirectional bus, transferring data to and from the device and peripherals. The outputs are tri-state buffers capable of driving one standard TTL load and 130 pF.

Ready (RDY)

This input signal allows the user to halt or single step the microprocessor on all cycles. A negative transition to the low state during or coincident with phase one (ϕ_1) will halt the microprocessor with the output address lines reflecting the current address being accessed. During a Write cycle the data bus will reflect the current data being written.

While RDY is low the CPU is in a low power mode.

Bus Enable (BE)

The BE input allows an external device to tri-state the address, data, and R/W lines by taking this line to a logical zero state.

Interrupt Request ($\overline{IRQ}$)

This TTL level input requests that an interrupt sequence begin within the microprocessor. The microprocessor will complete the instruction being executed before recognizing the request. At that time, the interrupt mask bit in the Status Code Register will be examined. If the interrupt mask flag is not set, the microprocessor will begin an interrupt sequence. The Program Counter and Processor Status Register are stored in the stack. The microprocessor will then set the interrupt mask flag high so that no further interrupts may occur. At the end of this cycle, the program counter low will be loaded from address FFFE and program counter high from location FFFF, thus transferring program control to the memory vector located at these addresses. The RDY signal must be in the high state for any interrupt to be recognized. An external pull-up resistor should be used for proper wire-OR operation.

Non-Maskable Interrupt ($\overline{NMI}$)

A negative going edge on this input requests that a non-maskable interrupt sequence be generated within the microprocessor.

$\overline{NMI}$ is an unconditional interrupt. Following completion of the current instruction, the sequence of operations defined for $\overline{IRQ}$ will be performed, regardless of the state of the interrupt mask flag. The vector address loaded into the program counter, low and high, are locations FFFA and FFFB respectively, thereby transferring program control to the memory vector located at these addresses. The instructions loaded at these locations cause the microprocessor to branch to a non-maskable interrupt routine in memory.

$\overline{NMI}$ requires an external resistor to V_{CC} for proper wire-OR operations.

Inputs $\overline{IRQ}$ and $\overline{NMI}$ are hardware interrupts lines sampled during ϕ_2 (phase 2). They begin the appropriate interrupt routine on the ϕ_1 (phase 1) following the completion of the current instruction.

Set Overflow Flag (S.O.)

A negative going edge on this input sets the overflow bit in the Status Code Register. This signal is sampled on the trailing edge of ϕ_1 and must be externally synchronized.

SYNC

This output line identifies those cycles in which the microprocessor is doing an OP CODE fetch. The SYNC line goes high during ϕ_1 of an OP CODE fetch and stays high for the remainder of that cycle. If the RDY line is pulled low during the ϕ_1 clock pulse in which SYNC went high, the processor will stop in its current state and will remain there until the RDY line goes high. In this manner the SYNC signal can be used to control RDY to cause single instruction execution.

Reset

This input resets or starts the microprocessor from a power down condition. During the time that this line is held low, writing to or from the microprocessor is inhibited. When a positive edge is detected on the input, the microprocessor will immediately begin the reset sequence.

After a system initialization time of six clock cycles, the mask interrupt flag will be set and the microprocessor will load the program counter from the memory vector locations FFFC and FFFD. This is the start location for program control.

This line is a Schmitt trigger input which facilitates the use of an RC network as a power on reset circuit.

Memory Lock ($\overline{ML}$)

This output may be used by external bus arbitration circuitry to avoid the interruption of read-modify-write instructions. These instructions are ASL, DEC, INC, LSR, RMB, ROR, SMB, TRB, and TSB.

ADDRESSING MODES

ACCUMULATOR ADDRESSING—This form of addressing is represented with a one byte instruction, implying an operation on the accumulator.

IMMEDIATE ADDRESSING—In immediate addressing, the second byte of the instruction contains the operand, with no further memory addressing required.

ABSOLUTE ADDRESSING—In absolute addressing, the second byte of the instruction specifies the eight low order bits of the effective address while the third byte specifies the eight high order bits. Thus, the absolute addressing mode allows access to the entire 64K bytes of addressable memory.

ZERO PAGE ADDRESSING—The zero page instructions allow for shorter code and execution times by fetching only the second byte of the instruction and assuming a zero high address byte. Careful use of the zero page can result in significant increase in code efficiency.

INDEXED ZERO PAGE ADDRESSING—(X, Y indexing)—This form of addressing is used with the index register and is referred to as "Zero Page, X" or "Zero Page, Y". The effective address is calculated by adding the second byte to the contents of the index register. Since this is a form of "Zero Page" addressing, the content of the second byte references a location in page zero. Additionally, due to the "Zero Page" addressing nature of this mode, no carry is added to the high order eight bits of memory and crossing of page boundaries does not occur.

INDEXED ABSOLUTE ADDRESSING—(X, Y indexing)—This form of addressing is used in conjunction with X and Y index register and is referred to as "Absolute, X" and "Absolute, Y". The effective address is formed by adding the contents of X or Y to the address contained in the second and third bytes of the instruction. This mode allows the index register to contain the index or count value and the instruction to contain the base address. This type of indexing allows any location referencing and the index to modify multiple fields, resulting in reduced coding and execution time.

NEW **INDEXED ABSOLUTE INDIRECT**—(new addressing mode—JMP (IND), X)—The contents of the second and third instruction bytes are added to the X-register. The sixteen-bit result is a memory address containing the effective address.

IMPLIED ADDRESSING—In the implied addressing mode, the address containing the operand is implicitly stated in the operation code of the instruction.

RELATIVE ADDRESSING—Relative addressing is used only with branch instructions and establishes a destination for the conditional branch.

The second byte of the instruction becomes the operand which is an "Offset" added to the contents of the lower eight bits of the program counter when the counter is set at the next instruction. The range of the offset is −128 to +127 bytes from the next instruction.

INDEXED INDIRECT ADDRESSING—In indexed indirect addressing (referred to as (Indirect, X)), the second byte of the instruction is added to the contents of the X index register, discarding the carry. The result of this addition points to a memory location on page zero whose contents are the low order eight bits of the effective address. The next memory location in page zero contains the high order eight bits of the effective address. Both memory locations specifying the high and low order bytes of the effective address must be in page zero.

INDIRECT INDEXED ADDRESSING—In indirect indexed addressing (referred to as (Indirect), Y), the second byte of the instruction points to a memory location in page zero. The contents of this memory location are added to the contents of the Y index register, the result being the low order eight bits of the effective address. The carry from this addition is added to the contents of the next page zero memory location, the result being the high order eight bits of the effective address.

ABSOLUTE INDIRECT—The second byte of the instruction contains the low order eight bits of a memory location. The high order eight bits of that memory location are contained in the third byte of the instruction. The contents of the fully specified memory location are the low order byte of the effective address. The next memory location contains the high order byte of the effective address which is loaded into the sixteen bits of the program counter. (JMP (IND) only)

INDIRECT—(new addressing mode)—The second byte of the instruction contains a zero page address serving as the indirect pointer.

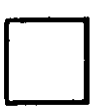
INSTRUCTION SET ALPHABETIC SEQUENCE

Mnemonic		Function
(2)	ADC	Add Memory to Accumulator with Carry
(2)	AND	"AND" Memory with Accumulator
	ASL	Shift Left One Bit (Memory or Accumulator)
(1)	BBR	Branch on Bit Reset
(1)	BBS	Branch on Bit Set
	BCC	Branch on Carry Clear
	BCS	Branch on Carry Set
	BEQ	Branch on Result Zero
(2)	BIT	Test Bits in Memory with Accumulator
	BMI	Branch on Result Minus
	BNE	Branch on Result not Zero
	BPL	Branch on Result Plus
(1)	BRA	Branch Always
	BRK	Force Break
	BVC	Branch on Overflow Clear
	BVS	Branch on Overflow Set
	CLC	Clear Carry Flag
	CLD	Clear Decimal Mode
	CLI	Clear Interrupt Disable Bit
	CLV	Clear Overflow Flag
(2)	CMP	Compare Memory and Accumulator
	CPX	Compare Memory and Index X
	CPY	Compare Memory and Index Y
(2)	DEC	Decrement Memory by One
	DEX	Decrement Index X by One
	DEY	Decrement Index Y by One
(2)	EOR	"Exclusive-OR" Memory with Accumulator
(2)	INC	Increment Memory by One
	INX	Increment Index X by One
	INY	Increment Index Y by One
(2)	JMP	Jump to New Location
	JSR	Jump to New Location Saving Return Address
(2)	LDA	Load Accumulator with Memory
	LDX	Load Index X with Memory
	LDY	Load Index Y with Memory
	LSR	Shift One Bit Right (Memory or Accumulator)
	NOP	No Operation
(2)	ORA	"OR" Memory with Accumulator
	PHA	Push Accumulator on Stack
	PHP	Push Processor Status on Stack
(1)	PHX	Push X Register on Stack
(1)	PHY	Push Y Register on Stack
	PLA	Pull Accumulator from Stack
	PLP	Pull Processor Status from Stack
(1)	PLX	Pull X Register from Stack
(1)	PLY	Pull Y Register from Stack
(1)	RMB	Reset Memory Bit
	ROL	Rotate One Bit Left (Memory or Accumulator)
	ROR	Rotate One Bit Right (Memory or Accumulator)
	RTI	Return from Interrupt
	RTS	Return from Subroutine
	SBC	Subtract Memory from Accumulator with Borrow
	SEC	Set Carry Flag
	SED	Set Decimal Mode
	SEI	Set Interrupt Disable Status
(1)	SMB	Set Memory Bit
(2)	STA	Store Accumulator in Memory
	STX	Store Index X in Memory
	STY	Store Index Y in Memory
(1)	STZ	Store Zero
	TAX	Transfer Accumulator to Index X
	TAY	Transfer Accumulator to Index Y
(1)	TRB	Test and Reset Bits
(1)	TSB	Test and Set Bits
	TSX	Transfer Stack Pointer to Index X
	TXA	Transfer Index X to Accumulator
	TXS	Transfer Index X to Stack Register
	TYA	Transfer Index Y to Accumulator

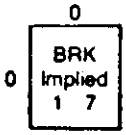
NOTES:
(1) New Instruction
(2) Previous Instruction with additional addressing mode(s)

INSTRUCTION SET OP CODE MATRIX

MSD \ LSD	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	MSD
0	BRK Implied 1 7	ORA (IND, X) 2 6	·		TSB ZP 2 5	ORA ZP 2 3	ASL ZP 2 5	RMB0 ZP 2 5	PHP Implied 1 3	ORA IMM 2 2	ASL Accum 1 2		TSB ABS 3 6	ORA ABS 3 4	ASL ABS 3 6	BBR0 ZP 3 5**	0
1	BPL Relative 2 2**	ORA (IND), Y 2 5*	ORA (IND) 2 5		TRB ZP 2 5	ORA ZP, X 2 4	ASL ZP, X 2 6	RMB1 ZP 2 5	CLC Implied 1 2	ORA ABS, Y 3 4*	INC Accum 1 2		TRB ABS 3 6	ORA ABS, X 3 4*	ASL ABS, X 3 7	BBR1 ZP 3 5**	1
2	JSR Absolute 3 6	AND (IND, X) 2 6			BIT ZP 2 3	AND ZP 2 3	ROL ZP 2 5	RMB2 ZP 2 5	PLP Implied 1 4	AND IMM 2 2	ROL Accum 1 2		BIT ABS 3 4	AND ABS 3 4	ROL ABS 3 6	BBR2 ZP 3 5**	2
3	BMI Relative 2 2**	AND (IND), Y 2 5*	AND (IND) 2 5		BIT ZP, X 2 4	AND ZP, X 2 4	ROL ZP, X 2 6	RMB3 ZP 2 5	SEC Implied 1 2	AND ABS, Y 3 4*	DEC Accum 1 2		BIT ABS, X 3 4*	AND ABS, X 3 4*	ROL ABS, X 3 7	BBR3 ZP 3 5**	3
4	RTI Implied 1 6	EOR (IND, X) 2 6				EOR ZP 2 3	LSR ZP 2 5	RMB4 ZP 2 5	PHA Implied 1 3	EOR IMM 2 2	LSR Accum 1 2		JMP ABS 3 3	EOR ABS 3 4	LSR ABS 3 6	BBR4 ZP 3 5**	4
5	BVC Relative 2 2**	EOR (IND), Y 2 5*	EOR (IND) 2 5			EOR ZP, X 2 4	LSR ZP, X 2 6	RMB5 ZP 2 5	CLI Implied 1 2	EOR ABS, Y 3 4*	PHY Implied 1 2			EOR ABS, X 3 4*	LSR ABS, X 3 7	BBR5 ZP 3 5**	5
6	RTS Implied 1 6	ADC (IND, X) 2 6†			STZ ZP 2 3	ADC ZP 2 3†	ROR ZP 2 5	RMB6 ZP 2 5	PLA Implied 1 4	ADC IMM 2 2†	ROR Accum 1 2		JMP Indirect 3 5	ADC ABS 3 4†	ROR ABS 3 6	BBR6 ZP 3 5**	6
7	BVS Relative 2 2**	ADC (IND), Y 2 5*†	ADC (IND) 2 5†		STZ ZP, X 2 4	ADC ZP, X 2 4†	ROR ZP, X 2 6	RMB7 ZP 2 5	SEI Implied 1 2	ADC ABS, Y 3 4*†	PLY Implied 1 2		JMP (IND), X 3 6	ADC ABS, X 3 4*†	ROR ABS, X 3 7	BBR7 ZP 3 5**	7
8	BRA Relative 2 3	STA (IND, X) 2 6			STY ZP 2 3	STA ZP 2 3	STX ZP 2 3	SMB0 ZP 2 5	DEY Implied 1 2	BIT IMM 2 2	TXA Implied 1 2		STY ABS 3 4	STA ABS 3 4	STX ABS 3 4	BBS0 ZP 3 5**	8
9	BCC Relative 2 2**	STA (IND), Y 2 6	STA (IND) 2 6		STY ZP, X 2 4	STA ZP, X 2 4	STX ZP, Y 2 4	SMB1 ZP 2 5	TYA Implied 1 2	STA ABS, Y 3 5	TXS Implied 1 2		STZ ABS 3 4	STA ABS, X 3 5	STZ ABS, X 3 5	BBS1 ZP 3 5**	9
A	LDY IMM 2 2	LDA (IND, X) 2 6	LDX IMM 2 2		LDY ZP 2 3	LDA ZP 2 3	LDX ZP 2 3	SMB2 ZP 2 5	TAY Implied 1 2	LDA IMM 2 2	TAX Implied 1 2		LDY ABS 3 4	LDA ABS 3 4	LDX ABS 3 4	BBS2 ZP 3 5**	A
B	BCS Relative 2 2**	LDA (IND), Y 2 5*	LDA (IND) 2 5		LDY ZP, X 2 4	LDA ZP, X 2 4	LDX ZP, Y 2 4	SMB3 ZP 2 5	CLV Implied 1 2	LDA ABS, Y 3 4*	TSX Implied 1 2		LDY ABS, X 3 4*	LDA ABS, X 3 4*	LDX ABS, Y 3 4*	BBS3 ZP 3 5**	B
C	CPY IMM 2 2	CMP (IND, X) 2 6			CPY ZP 2 3	CMP ZP 2 3	DEC ZP 2 5	SMB4 ZP 2 5	INY Implied 1 2	CMP IMM 2 2	DEX Implied 1 2		CPY ABS 3 4	CMP ABS 3 4	DEC ABS 3 6	BBS4 ZP 3 5**	C
D	BNE Relative 2 2**	CMP (IND), Y 2 5*	CMP (IND) 2 5			CMP ZP, X 2 4	DEC ZP, X 2 6	SMB5 ZP 2 5	CLD Implied 1 2	CMP ABS, Y 3 4*	PHX Implied 1 2			CMP ABS, X 3 4*	DEC ABS, X 3 7	BBS5 ZP 3 5**	D
E	CPX IMM 2 2	SBC (IND, X) 2 6†			CPX ZP 2 3	SBC ZP 2 3†	INC ZP 2 5	SMB6 ZP 2 5	INX Implied 1 2	SBC IMM 2 2†	NOP Implied 1 2		CPX ABS 3 4	SBC ABS 3 4†	INC ABS 3 6	BBS6 ZP 3 5**	E
F	BEQ Relative 2 2**	SBC (IND), Y 2 5*†	SBC (IND) 2 5†			SBC ZP, X 2 4†	INC ZP, X 2 6	SMB7 ZP 2 5	SED Implied 1 2	SBC ABS, Y 3 4*†	PLX Implied 1 2			SBC ABS, X 3 4*†	INC ABS, X 3 7	BBS7 ZP 3 5**	F
	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	



— New Opcode



—OP Code
—Addressing Mode
—Instruction Bytes; Machine Cycles

†Add 1 to N if in decimal mode.
*Add 1 to N if page boundary is crossed.
**Add 1 to N if branch occurs to same page;
Add 2 to N if branch occurs to different page.

INSTRUCTION SUMMARY

MNEMONIC	OPERATION	IMMEDIATE OP	IMMEDIATE n	IMMEDIATE #	ABSOLUTE OP	ABSOLUTE n	ABSOLUTE #	ZERO PAGE OP	ZERO PAGE n	ZERO PAGE #	ACCUM OP	ACCUM n	ACCUM #	IMPLIED OP	IMPLIED n	IMPLIED #	(IND. X) OP	(IND. X) n	(IND. X) #	(IND). Y OP	(IND). Y n	(IND). Y #	Z PAGE, X OP	Z PAGE, X n	Z PAGE, X #	ABS. X OP	ABS. X n	ABS. X #	ABS. Y OP	ABS. Y n	ABS. Y #	RELATIVE OP	RELATIVE n	RELATIVE #	INDIRECT OP	INDIRECT n	INDIRECT #	Z PAGE, Y OP	Z PAGE, Y n	Z PAGE, Y #	BIT ADDRESSING (OP BY BIT #) 0	1	2	3	4	5	6	7	PROCESSOR STATUS CODES 7	6	5	4	3	2	1	0
ADC	A + M + C → A (1) (5)	69	2	2	6D	4	3	65	3	2							61	6	2	71	5	2	75	4	2	7D	4	3	79	4	3				72	5	2													N	V	·	·	·	·	Z	C
AND	A M → A (1)	29	2	2	2D	4	3	25	3	2							21	6	2	31	5	2	35	4	2	3D	4	3	39	4	3				32	5	2													N	·	·	·	·	·	Z	·
ASL	C ← [7 6 5 4 3 2 1 0] ← 0				0E	6	3	06	5	2	0A	2	1										16	6	2	1E	7	3																					N	·	·	·	·	·	Z	C
BBR#(#=0-7)	Branch on M_6 = 0 (4)																																						0F	1F	2F	3F	4F	5F	6F	7F												
BBS#(#=0-7)	Branch on M_6 = 1 (4)																																						8F	9F	AF	BF	CF	DF	EF	FF												
BCC	Branch on C = 0 (2)																														90	2	2																												
BCS	Branch on C = 1 (2)																														B0	2	2																												
BEQ	Branch on Z = 1 (2)																														F0	2	2																												
BIT	A AND M	89	2	2	2C	4	3	24	3	2													34	4	2	3C	4	3																					M$_7$	M$_6$	·	·	·	·	Z	·
BMI	Branch on N = 1 (2)																														30	2	2																												
BNE	Branch on Z = 0 (2)																														D0	2	2																												
BPL	Branch on N = 0 (2)																														10	2	2																												
BRA	Branch Always (2)																														80	2	2																												
BRK	Break (See Fig. 1)													00	7	1																																															
BVC	Branch on V = 0 (2)																														50	2	2																												
BVS	Branch on V = 1 (2)																														70	2	2																												
CLC	0 → C													18	2	1																																														
CLD	0 → D													D8	2	1																																													
CLI	0 → I													58	2	1																																													
CLV	0 → V													B8	2	1																																													
CMP	A M	C9	2	2	CD	4	3	C5	3	2							C1	6	2	D1	5	2	D5	4	2	DD	4	3	D9	4	3				D2	5	2													N	N	·	·	·	·	Z	C
CPX	X M	E0	2	2	EC	4	3	E4	3	2																																											N	N	·	·	·	·	Z	C
CPY	Y M	C0	2	2	CC	4	3	C4	3	2																																											N	N	·	·	·	·	Z	C
DEC	M - 1 → M				CE	6	3	C6	5	2	3A	2	1										D6	6	2	DE	7	3																					N	N	·	·	·	·	Z	·
DEX	X - 1 → X													CA	2	1																																			N	N	·	·	·	·	Z	·
DEY	Y - 1 → Y													88	2	1																																			N	N	·	·	·	·	Z	·
EOR	A VM → A (1)	49	2	2	4D	4	3	45	3	2							41	6	2	51	5	2	55	4	2	5D	4	3	59	4	3				52	5	2													N	N	·	·	·	·	Z	·
INC	M + 1 → M				EE	6	3	E6	5	2	1A	2	1										F6	6	2	FE	7	3																					N	N	·	·	·	·	Z	·
INX	X + 1 → X													E8	2	1																																			N	N	·	·	·	·	Z	·
INY	Y + 1 → Y													C8	2	1																																			N	N	·	·	·	·	Z	·
JMP	Jump to New Loc				4C	3	3																													6C	6	3													·	·	·	·	·	·	·	·
JSR	Jump Sub (See Fig. 2)				20	6	3																																																						
LDA	M → A (1)	A9	2	2	AD	4	3	A5	3	2							A1	6	2	B1	5	2	B5	4	2	BD	4	3	B9	4	3				B2	5	2													N	·	·	·	·	·	Z	·
LDX	M → X (1)	A2	2	2	AE	4	3	A6	3	2																													BE	4	3	B6	4	2								N	N	·	·	·	·	Z	·
LDY	M → Y (1)	A0	2	2	AC	4	3	A4	3	2													B4	4	2	BC	4	3																					N	N	·	·	·	·	Z	·
LSR	0 → [7 6 5 4 3 2 1 0] → C				4E	6	3	46	5	2	4A	2	1										56	6	2	5E	7	3																					0	·	·	·	·	·	Z	C
NOP	No Operation													EA	2	1																																			·	·	·	·	·	·	·	·
ORA	A VM → A	09	2	2	0D	4	3	05	3	2							01	6	2	11	5	2	15	4	2	1D	4	3	19	4	3				12	5	2													N	·	·	·	·	·	Z	·
PHA	A → Ms S - 1 → S													48	3	1																																			·	·	·	·	·	·	·	·
PHP	P → Ms S - 1 → S													08	3	1																																			·	·	·	·	·	·	·	·
PHX	X → Ms S - 1 → S													DA	3	1																																			·	·	·	·	·	·	·	·
PHY	Y → Ms S - 1 → S													5A	3	1																																			·	·	·	·	·	·	·	·
PLA	S + 1 → S Ms → A													68	4	1																																			N	·	·	·	·	·	Z	·
PLP	S + 1 → S Ms → P													28	4	1																																			(Restored)							
PLX	S + 1 → S Ms → X													FA	4	1																																			·	·	·	·	·	·	·	·
PLY	S + 1 → S Ms → Y													7A	4	1																																			·	·	·	·	·	·	·	·
RMB#(#=0-7)	0 → M_6 (5)																																																										
ROL	[7 6 5 4 3 2 1 0] ← C				2E	6	3	26	5	2	2A	2	1										36	6	2	3E	7	3																					N	·	·	·	·	·	Z	C
ROR	C → [7 6 5 4 3 2 1 0]				6E	6	3	66	5	2	6A	2	1										76	6	2	7E	7	3																					N	·	·	·	·	·	Z	C
RTI	Return Int (See Fig. 1)													40	6	1																																			(Restored)							
RTS	Return Sub (See Fig. 2)													60	6	1																																			·	·	·	·	·	·	·	·
SBC	A M C → A (1) (5)	E9	2	2	ED	4	3	E5	3	2							E1	6	2	F1	5	2	F5	4	2	FD	4	3	F9	4	3				F2	5	2													N	V	·	·	·	·	Z	(3)
SEC	1 → C													38	2	1																																			·	·	·	·	·	·	·	1
SED	1 → D													F8	2	1																																			·	·	·	·	·	·	·	·
SEI	1 → I													78	2	1																																			·	·	·	·	·	·	·	·
SMB#(#=0-7)	1 → M_6 (4)																																																									
STA	A → M				8D	4	3	85	3	2							81	6	2	91	6	2	95	4	2	9D	5	3	99	5	3				92	5	2													·	·	·	·	·	·	·	·
STX	X → M				8E	4	3	86	3	2																													96	4	2												·	·	·	·	·	·	·	·
STY	Y → M				8C	4	3	84	3	2													94	4	2																										·	·	·	·	·	·	·	·
STZ	0 → M				9C	4	3	64	3	2													74	4	2	9E	5	3																					·	·	·	·	·	·	·	·
TAX	A → X													AA	2	1																																			N	·	·	·	·	·	Z	·
TAY	A → Y													A8	2	1																																			N	·	·	·	·	·	Z	·
TRB	A ∧ M → M				1C	6	3	14	5	2																																										M	M$_6$	·	·	·	·	Z	·
TSB	A V M → M				0C	6	3	04	5	2																																										M	M$_6$	·	·	·	·	Z	·
TSX	S → X													BA	2	1																																			N	·	·	·	·	·	Z	·
TXA	X → A													8A	2	1																																			N	·	·	·	·	·	Z	·
TXS	X → S													9A	2	1																																			·	·	·	·	·	·	·	·
TYA	Y → A													98	2	1																																			N	·	·	·	·	·	Z	·

NOTES

1. Add 1 to N if page boundary is crossed
2. Add 1 to N if branch occurs to same page
   Add 2 to N if branch occurs to different page
3. Carry not = Borrow
4. Effects 8-bit data field of the specified zero page address
5. Add 1 to N if in Decimal Mode

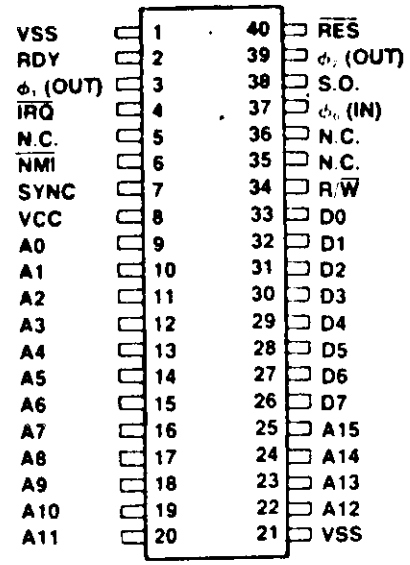
LEGEND

X	= Index X	M_6	= Memory Bit 6
Y	= Index Y	+	= Add
A	= Accumulator	-	= Subtract
M	= Memory per effective address	∧	= And
M_s	= Memory per stack pointer	V	= Or
M_b	= Selected zero page memory bit	V	= Exclusive or
M_7	= Memory Bit 7	N	= Number of cycles
		#	= Number of Bytes

HARDWARE SPECIFICATIONS

R65C02—40 Pin Package

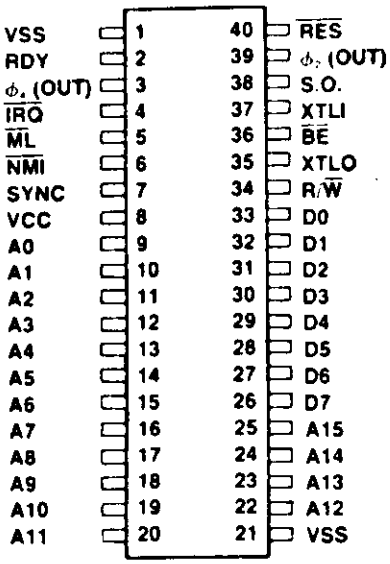
Pin Outs



FEATURES

- Pin Compatible with NMOS R6502
- 64K Addressable Bytes of Memory (A0-A15)
- IRQ Interrupt
- On-the-chip Clock
  —TTL Level Single Phase Input
- SYNC Signal
  (can be used for single instruction execution)
- RDY Signal
  (can be used to halt or single cycle execution)
- Two Phase Output Clock for Timing of Support Chips
- NMI Interrupt

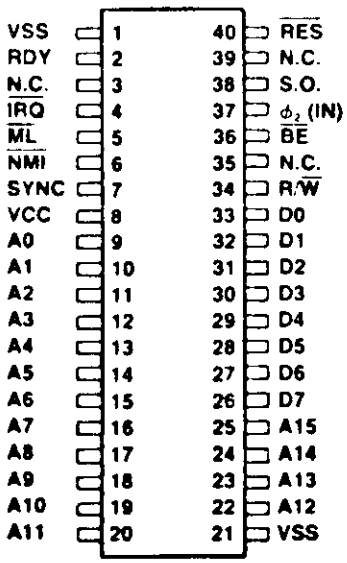
R65C102—40 Pin Package



FEATURES

- Φ1 Quadrature Clock Output eases access time requirements
- 64K Addressable Bytes of Memory (A0-A15)
- IRQ Interrupt
- On-the-chip Clock
  —TTL Level Single Phase Input
  —RC Time Base Input
  —Crystal Time Base Input (÷ 4)
- SYNC Signal (can be used for signal instruction execution)
- RDY Signal (can be used to halt or single cycle execution)
- Two Phase Output Clock for Timing of Support Chips
- NMI Interrupt
- Direct Memory Access Capability
- Memory Lock Output
- Bus Enable Signal

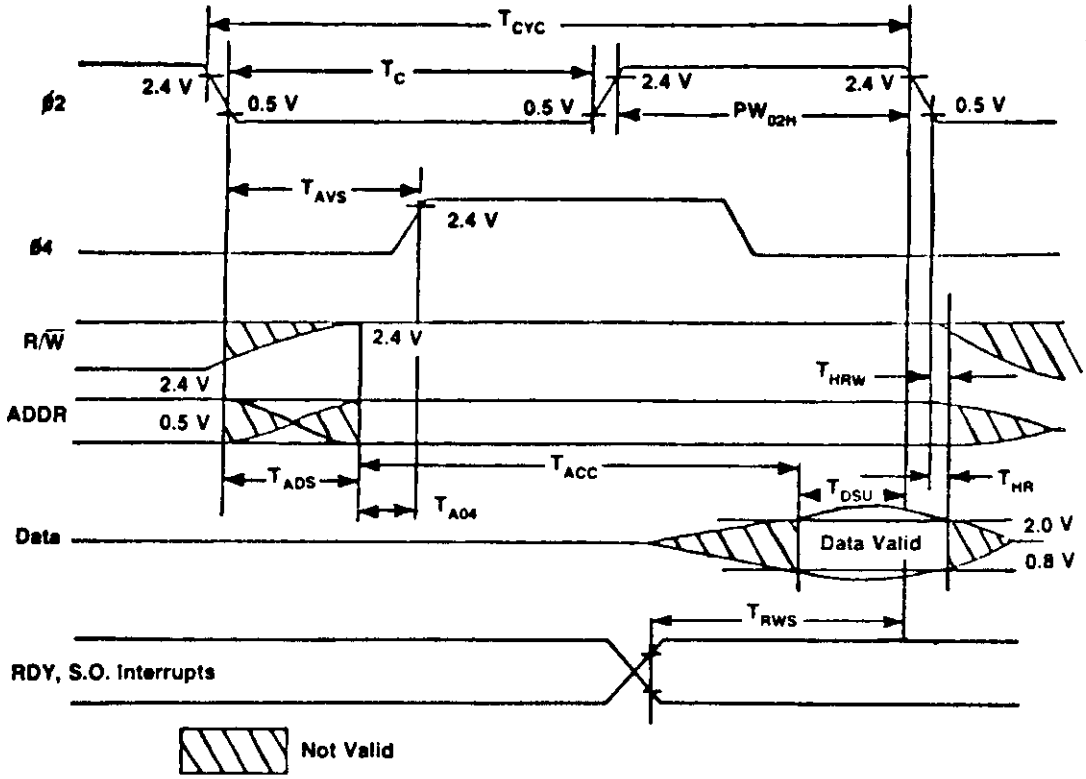
R65C112—40 Pin Package



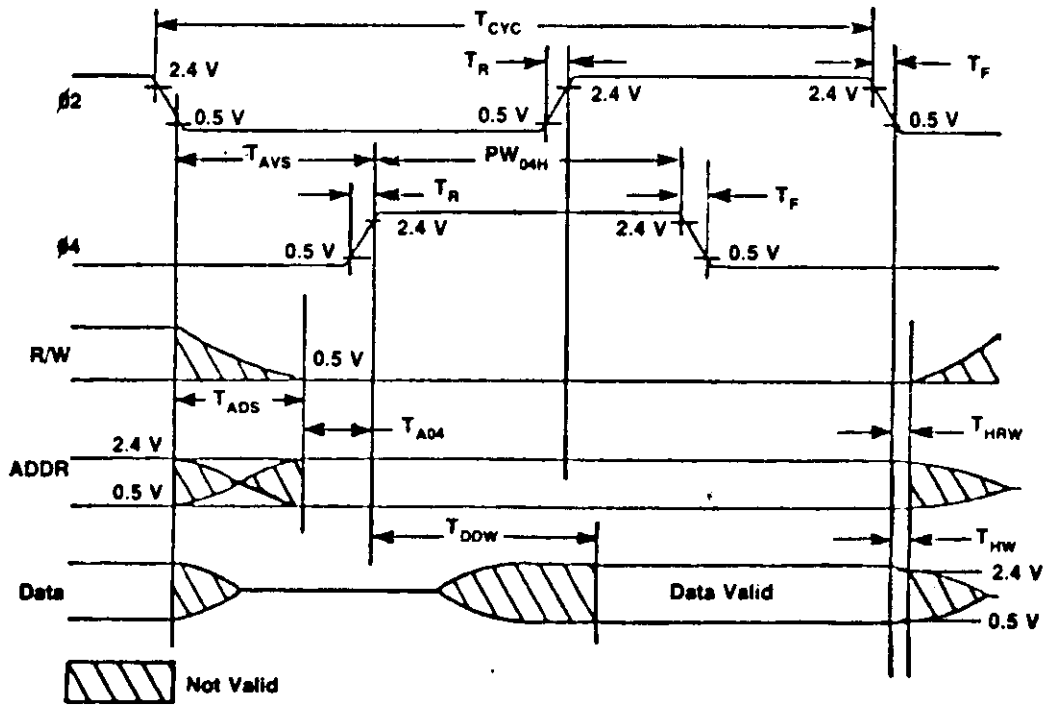
FEATURES

- Slave Processor Version
- 64K Addressable Bytes of Memory (A0-A15)
- IRQ Interrupt
- NMI Interrupt
- RDY Signal
- 8 Bit Bidirectional Data Bus
- SYNC and RDY Signal
- Two phase clock input
- Bus Enable
- Direct Memory Access capability
- Memory Lock Output

READ DATA FROM MEMORY OR PERIPHERALS TIMING



WRITE DATA TO MEMORY OR PERIPHERALS TIMING



*Hold time for BA, BS not specified

A.C. Electrical Timing Characteristics

Characteristic	Symbol	2MHz		3MHz		4MHz		Units
		Min	Max	Min	Max	Min	Max	
Cycle Time	T_{CYC}	500		333		250		ns
Pulse Width, 02 Low	PW_{02L}	210		160		100		ns
Pulse Width, 02 High	PW_{02H}	220		170		110		ns
Clock Rise & Fall Time	T_R, T_F		15		12		10	ns
Pulse Width, 04 Low	PW_{04L}	210		150		100		ns
Pulse Width, 04 High	PW_{04H}	220		160		110		ns
Delay Time 02 to 04 Rise	T_{AVS}	80	125		94		63	ns
Address Delay	T_{ADS}		100		75		50	ns
Address Hold Time (Address, R/W)	T_{HRW}	20		20		20		ns
Address Valid to 04 Rise	T_{A04}	25		18		12		ns
Data Delay Time (Write)	T_{DDW}		110		82		55	ns
Read Data Setup Time	T_{DSU}	40		30		20		ns
Read Data Hold Time	T_{HR}	10		10		10		ns
Write Data Hold Time	T_{HW}	30		30		30		ns
Read Access Time	T_{ACC}	340		254		168		ns
Processor Control Setup Time (RDY, S.O. Interrupts, Reset)	T_{RWS}	110		80		60		ns
Bus Enable Setup Time	T_{BE}	125		100		75		ns

D.C. CHARACTERISTICS

Maximum Ratings

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.3 to +7.0	Vdc
Input Voltage	V_{in}	-0.3 to +7.0	Vdc
Operating Temperature	T		°C
Commercial		0 to +70	
Industrial		-40 to +85	
Storage Temperature	T_{STG}	-55 to +150	°C

NOTE

This device contains input protection against damage to high static voltages or electric fields; however, precautions should be taken to avoid application of voltages higher than maximum rating.

Electrical Characteristics

(V_{CC} = 5.0 ±20%, V_{SS} = 0)

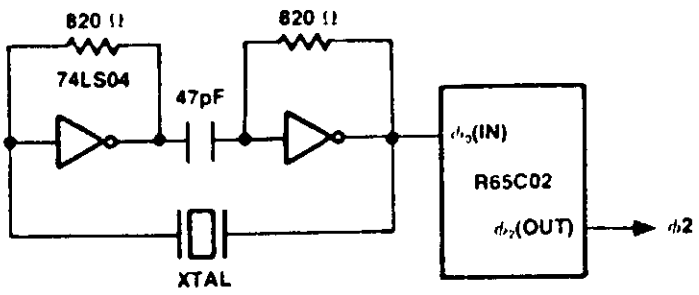
Characteristic	Symbol	Min	Max	Unit
Input High Voltage All Input Pins (except ϕ_2 on R65C112)	V_{IH}	2.0	V_{CC} + 0.3	Vdc
Input Low Voltage All Input Pins (except ϕ_2 on R65C112)	V_{IL}	-0.3	0.8	Vdc
Input High Voltage $\phi_{2\ in}$ on R65C112	V_{IH}	2.4	—	Vdc
Input Low Voltage $\phi_{2\ in}$ on R65C112	V_{IL}	—	0.4	Vdc
Input Leakage Current (V_{in} = 0 to 5.25V, V_{CC} = 0) Logic (Excl. Rdy, S.O.) ϕ_1, ϕ_2 $\phi_{o(in)}$	I_{in}	— — —	1.0 1.0 1.0	μA
Three-State (Off State) Input Current (V_{in} = 0.4 to 2.4V, V_{CC} = 5.25V) Data Lines	I_{TSI}	—	10	μA
Output High Voltage (I_{LOAD} = -100 μAdc, V_{CC} = 4.75V) SYNC, Data, A0-A15, R/$\overline{W}$, ϕ_1, ϕ_2	V_{OH}	V_{SS} + 2.4	—	Vdc
Output Low Voltage (I_{LOAD} = 1.6 mAdc, V_{CC} = 4.75V) SYNC, Data, A0-A15, R/$\overline{W}$, ϕ_1, ϕ_2	V_{OL}		V_{SS} + 0.4	Vdc
Power Dissipation 0 MHz (Standby) 1 MHz 2 MHz 3 MHz 4 MHz Low Power (RDY = 0)	P_D	— —	10 20 40 60 80 10	μW mW mW/MHz
Capacitance at 25°C (V_{in} = 0, f = 1 MHz Logic Data A0-A15, R/W, SYNC $\phi_{o(in)}$ ϕ_1 ϕ_2	C C_{in} C_{out} $C\phi_{o(in)}$ $C\phi_1$ $C\phi_2$	— — — — —	5 10 10 10 30 50	pF

NOTE

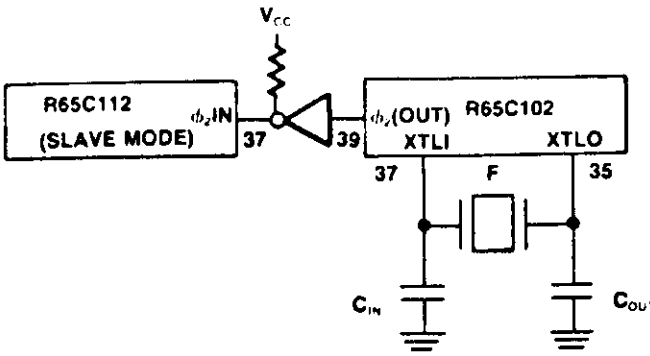
$\overline{IRQ}$ and $\overline{NMI}$ require external pull-up resistor.

CLOCK CONSIDERATIONS

EXAMPLE TIME BASE GENERATION



*CRYSTAL: CTS KNIGHTS MP SERIES, OR EQUIVALENT



F	CIN	COUT	ϕ_2
16 MHZ	16PF	16PF	4 MHZ
8 MHZ	18PF	18PF	2 MHZ
6 MHZ	20PF	20PF	1.5 MHZ
4 MHZ	24PF	24PF	1 MHZ

The oscillator in the R65C102 is series resonant.

The crystal input is divided by 4: (R65C102 ONLY)

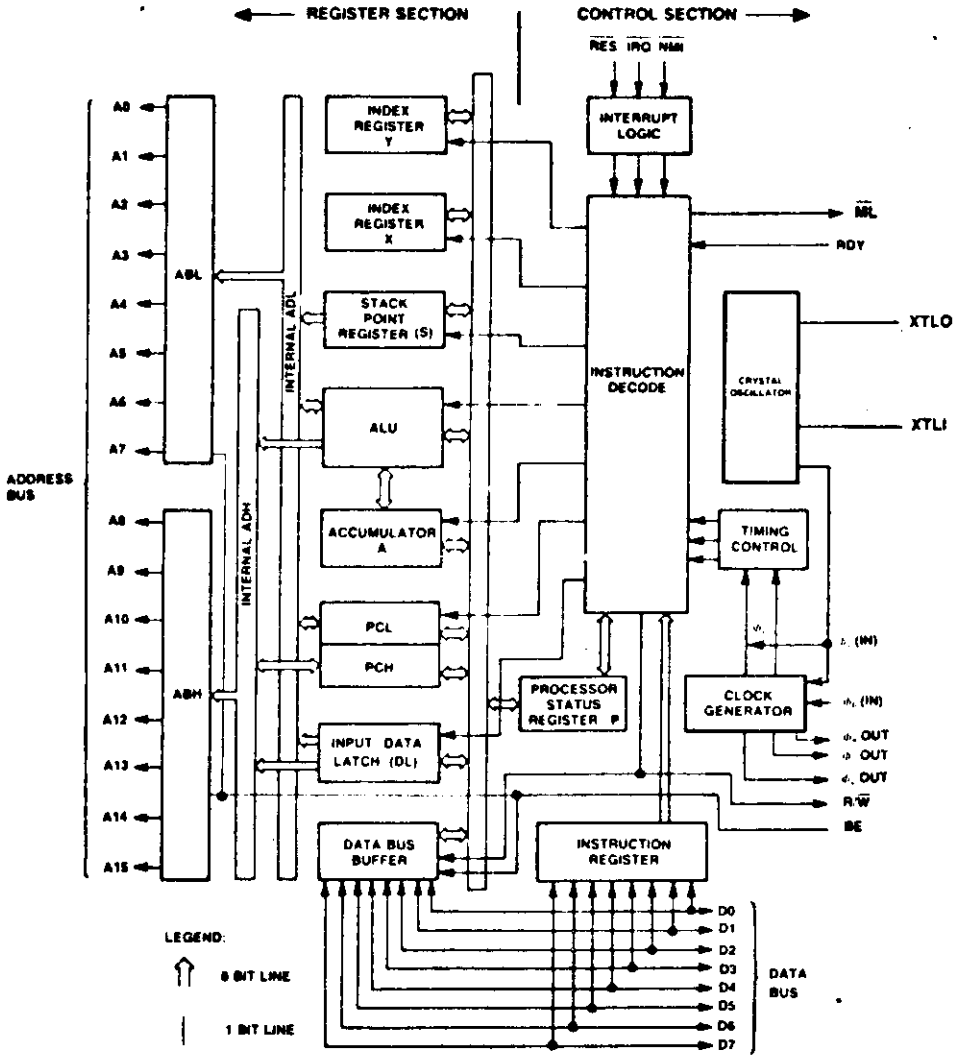
$$\phi_2 = \frac{XTAL}{4}$$

NOMINAL CRYSTAL PARAMETERS

	3.58	4.0	6.0	8.0	16.0	MHZ
RS	60	50	30-50	20-40	10-30	Ω
C0	3.5	6.5	4-6	4-6	3-5	PF
C1	.015	.025	.01-.02	.01-.02	.01-.02	PF
Q	740K	730K	720K	720K	720K	K

Note: These represent at-cut crystal parameters only. Others may be used.

R6500 INTERNAL ARCHITECTURE



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